5 Novel Switch Architectures

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Abstract: In this paper we discussed different switch architectures. We focus mainly on optical buffering. We investigate an all-optical buffer architecture comprising of cascaded stages of quantum-dot semiconductor optical amplifier-based tunable wavelength converters, at 160 Gb/s. We also propose the optical buffer with multi-wavelength converters based on quantum-dot semiconductor optical amplifiers. We present multistage switching fabrics with optical buffers, where optical buffers are based on fibre delay lines and are located in the first stage. Finally, we describe a photonic asynchronous packet switch and show that the employment of a few optical buffer stages to complement the electronic ones significantly improves the switch performance. We also propose two asynchronous optical packet switching node architectures, where an efficient contention resolution is based on controllable optical buffers and tunable wavelength converters TWCs.

5.1 Introduction

Optical fibres introduced in transmission systems offer a huge transmission bandwidth unavailable for copper cables. Transmission bit rates of 2.5, 10 and 40 Gb/s are now available and soon rates of 160 Gb/s will be available commercially. Electronic switching cannot be used at such high rates, so incoming signals have to be not only converted from optical to electrical form but also have to be demultiplexed to lower bit rates. To omit this inconvenient and expensive signal conversion and demultiplexing, switching systems based on the optical technology have been elaborated in research laboratories and industry. Optical switching, called also photonic switching, enables optical signals to be switched directly from inputs to outputs without conversion to electronic form. To construct optical switching elements, different technologies are being used. They exploit various optical effects in materials. In general, these technologies can be grouped into two main categories [1]: guided lightwave based switches and free-space switches. Each category can be further divided into different classes, depending on the

physical phenomena used to switch lightwaves between inputs and outputs. We can distinguish: electro-optic switches, acousto-optic switches, thermo-optic switches, MEMS switches, liquid-crystal switches, SOAs based switches. Detailed description of different technologies and examples of optical switching elements can be found in [1]. One of popular electro-optic switches is the titanium diffused lithium-niobate (Ti:$LiNbO_3$) directional coupler. It has a capacity of 2×2 and can be in one of two states: cross or bar. In MEMS technology switches may have different capacities (on-off switch, 2×2, $1 \times N$, $N \times N$) and different moving parts (mirrors, prisms, lenses, fibres).

Functions performed by an optical switching note are closely related to the transfer mode used in the optical transport network. At present, most optical nodes provide circuit switching either on the fibre level or wavelength level. These nodes are Optical Add/Drop Multiplexers (OADMs) and Optical Cross-Connects (OXCs). Different architectures of OADMs and OXCs were proposed in literature and implemented in practice [2]. Some of them use optical switching fabric to switch fibres or wavelengths. Examples of such architectures are shown in Fig. 5.5.1. OXCs and OADMs mostly used MEMS switches. This technology is relatively cheap and mature, however the switching time is rather slow, and cannot be used in Optical Packet Switches (OPS). Much faster switching elements are needed in OPS. However, fast optical switches are at the moment very expensive and not mature. The compromise between the circuit switching and packet switching is the Optical Burst Switching (OBS). OPS/OBS switches are considered for use in core routers [3, 4, 5].

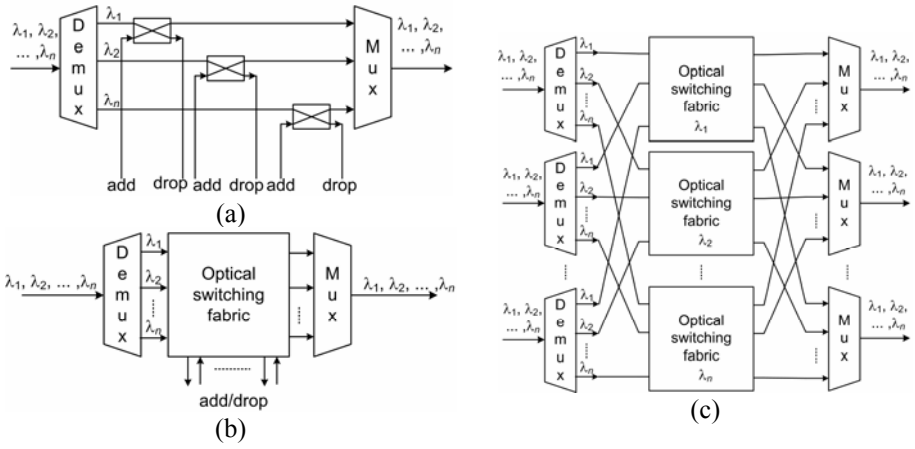


Fig. 5.1. (a) OADM with switching elements (b) OADM with the switching fabric (c) OXC with separate switching fabrics for each wavelength.

In packet (burst) switching one of the important functions of the switch it to solve the output contention problem. This contention appears when two or more packets are to be directed to the same output at the same time. The output contention can be solved in the space, wavelength, or time domains. In the space domain, one packet is directed to the desired output, while other competing packets are di-

rected to other outputs. This approach is also called the deflection routing. Such deflected packets can be directed back to their original destination in one of the next nodes. When wavelength multiplexing is used in the output ports, contention may be solved in wavelength domain by sending congested packets to the same output but on different wavelength. This requires the wavelength conversion capability in the switching node. Finally, when one of competing packets is sent to its original output, other congested packets are directed to the memory and delayed for some time.

The latter issue – buffering is an important functionality in optical burst-switched networks. It allows the temporal storing of data bursts or packets to resolve contention for the switch outputs. In case of all-optical buffering, we are facing a lack of RAM memory, wide available in electronics. Thus, electronic buffering has been extensively utilized in currently installed optical networks at a great cost and complexity and is limited by the electronic processing speeds and the relative slow O/E and E/O conversion times [6]. On the other hand, programmable fibre delay lines have been extensively used to form feed-forward [7] or recirculating schemes, employing in addition wavelength conversion to enhance buffering capabilities [8, 9, 10]. In particularly, feedback loops theoretically provide infinite storage time, but they suffer from noise accumulation and OSNR degradation. In contrast, feed-forward delay line buffers allow for short buffering times but recent studies indicate that statistically multiplexed optical networks will require only minimal buffering, provided some traffic engineering is performed [11]. Other storing technology such “slow light” are even more immature and up to date.

The paper gives some latest results in Optical Packet/Burst Switch architectures, with the special attention put on optical buffering. In Section 2 we demonstrate the applicability of QD-SOAs in an optical buffer architecture that can support ultra-high speed optical packet switching. Packet buffering is implemented in a multi-stage Time-Slot-Interchanger (TSI) that consists of quantum-dot semiconductor optical amplifiers (QD-SOAs) based wavelength converters exploiting the cross-gain modulation (XGM) effect and feed-forward delay lines. QD-SOAs constitute candidate technology for this purpose due to their advantageous properties such as strong nonlinearities, high gain and ultra-fast carrier dynamics which lies on the subpicosecond scale [12, 13] are heralded as the main technology able to support signal processing applications at high bit rates that reach up to 160 Gb/s.

A significant reduction in the number of active and passive components needed, can be achieved when using switches with multi-wavelength switching capabilities. QD-SOAs have been reported as a candidate technology to provide multi-wavelength operation at high bit rates [14]. Other technology candidate is acousto-optic tunable filters, [15], which are slower, with less flexibility in processing a multi-wavelength spectrum, but it is a proven technology. The switch architecture with QD-SOAs performing a multi-wavelength conversion is the subject of Section 3.

In Section 4 we describe an architecture of the single-stage shared-FDL switch and FDL assignment algorithms. Next we show how to build a multistage optical

switch using the single-stage shared-FDL switch. The architecture of the three-stage Clos-network is considered in our research as a potential solution to overcome the limited scalability of single-stage switches. Two FDLs assignment algorithms for the three-stage optical Clos-network are presented: sequential FDL assignment algorithm for Clos-network switches (SEFAC) and multicell FDL assignment for Clos-network switches (MUFAC). Furthermore, the results of simulation experiments are shown.

In Section 5 we describe a photonic asynchronous packet switch and show that the employment of a few optical buffer stages to complement the electronic ones significantly improves the switch performance. Furthermore we propose two asynchronous optical packet switching node architectures, where an efficient contention resolution is based on controllable optical buffers and tunable wavelength converters TWCs. First, we describe the new types of variable optical memory and evaluate the benefits of implementing them in the optical packet switching node. Furthermore, two structures of the switching node with dedicated and shared hybrid buffer respectively are presented along with two switching node architectures with contention resolution based on both buffering and wavelength conversion. We show that providing a few shared optical buffers significantly boosts the performance improvement obtained by TWCs.

5.2 Application of quantum-dot SOAs for the realization of all-optical buffer architectures up to 160 Gb/s

The buffer architecture comprises cascaded programmable delay stages, each consisting of two Tunable Wavelength Converters (TWCs) and two delay line banks. Each TWC provides *w* separate wavelengths at its output, and each wavelength is routed to the respective branch of the delay line bank by means of a wavelength demultiplexer. Adjacent TWCs and stages are connected by wavelength multiplexers. The system architecture has been designed based on [16] modified such as to utilize the maximum number of available wavelengths and it is presented in detail in [17].

Full wavelength utilization is of practical importance when considering QD-SOAs, since the devices exhibit a limited wavelength range due to the fact that wavelengths that do not reside in the same homogenous gain peak do not interact. Moreover, the channel spacing is many hundreds of GHz in systems that employ QD-SOA based TWCs, because of the ultra high rates that the devices are required to operate at (160 Gbps and beyond). The combined effects of the limited homogenous bandwidth and the increased wavelength spacing in high data rates mean that the total number of available wavelengths is drastically reduced in QD-SOA based TWCs when compared to the number of available wavelengths in conventional SOA and fibre based TWCs.

In buffer architectures, however, the number of available wavelengths determines the buffer storage capacity, and more wavelengths enable the design of buffers with increased buffering capabilities. On the contrary, if the number of available wavelengths is limited or if the available wavelengths are not optimally used, increased storage capacities will be realized at the expense of the buffer size. That is, more buffering stages are required in a multistage architecture, leading to increased system cost, as well as severe optical signal degradation due to the cascade of TWCs. Since QD-SOA based TWCs inherently lack a wide wavelength range, the buffer designer should focus on fully exploiting the number of wavelengths that are available by the QD-SOA. Moreover, the designer should pursue an architecture that minimizes the number of required stages for a given number of available wavelengths.

A well known multi-stage architecture that ensures minimization of the number of buffer stages is the Benes network. The principle of operation of the Benes network in buffering architectures is identical to its operation in space switches; still, Benes buffering involves the time-domain interchange of the packet positions, whereas Benes switching involves the spatial interchange of the packets. Under this scheme, if each Benes buffering stage is capable of interchanging n packets in total, then the i-th cascade stage must be able to interchange n packets that are spaced by ni packet durations (slots). In space switching terms this corresponds to having a Benes network that is formed from $n \times n$ switches: each switch has the capability of spatially interchanging n packets, while switches in stage i of the network interchange packets that are spaced ni positions apart.

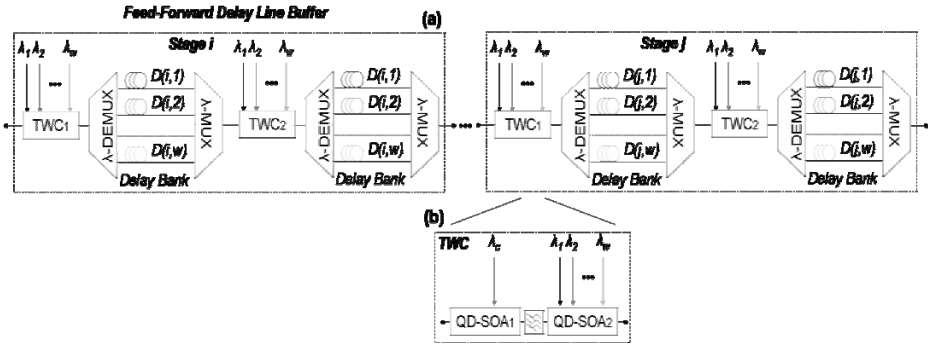


Fig. 5.2. (a) The structure of each delay stage. (b) The QDSOA tunable wavelength converter (TWC) setup. λ-MUX/DEMUX are the wavelength multiplexers and demultiplexers, respectively [17].

Following the above, the challenge is to design Benes packet interchanging stages that fully utilize the number of available wavelengths w provided by the QD-SOA based TWC SOAs. It has been shown in [17] that the maximum number of packets that can be interchanged per stage are $n = w - 1$. Even though the analysis is beyond the scope of the current chapter, it is easy to show that it is not

possible to utilize all available wavelengths by considering two packets and two wavelengths (n, $w = 2$). Clearly, there is no possible means of interchanging two successive packets in a Benes stage with two wavelengths, since the stage will provide delays that equal '0' or '1' packet durations only. Should the first packet be delayed by '1' packet duration, both packets will arrive simultaneously at the output of the delay line, therefore packet collision and consequent loss will occur. If the first packet is not delayed at all then interchanging cannot be performed. However, the two packets can be interchanged if three wavelengths are used, since an additional delay of '2' packet durations is available. By assigning first packet a '2' packet delay and the second packet a '0' delay, packet positions are interchanged at the output of the delay lines. Additionally, having a single TWC followed by w delay lines does not suffice to interchange all n packets. This is so, since interchanging packets 1 and n requires that packet 1 is delayed by $2n - 1$.This delay can only be achieved by cascading a second TWC with delay lines inside the Benes stage and the maximum delay in such case is $2(w - 1)$ or $2n$. Therefore the construction of the Benes stages results in a cascade of two TWCs plus delay lines per stage.

In agreement with the theoretical analysis, the main elements of TWC subsystem are two QD-SOAs in serial configuration as illustrated in Fig. 5.3(a). Wavelength conversion is performed in two steps based on the cross-gain modulation (XGM) effect between a data signal (pump) and a continuous wave signal (probe) in each QD-SOA, respectively. The incoming data signal modulates the carrier density and consequently the gain of the QD-SOA, resulting in the respective modulation of the cw probe signal which at the output of the QD-SOA has inverse polarity. Wavelength conversion from λ_m to λ_n is facilitated by intermediate conversion from λ_m to λ_c in QD-SOA1 and from λ_c to λ_n in QD-SOA2, where λ_c represents the center of the inhomogeneously broadened gain profile of the device. On one hand, the second QD-SOA is used to convert the signal polarity back to its initial state and on the other, to account for the case that the input data signal is not to be converted (in case this is defined by the routing algorithm) hence the cw wavelength needs to be different from the pump wavelength at each intermediate conversion. Furthermore, each QD-SOA is followed by a tunable optical filter aiming to cut off the unnecessary pump signal and keep only the modulated probe signal which will be fed into the next QD-SOA and play the role of the modulating pump. Finally, the saturable absorber is used to compensate for the extinction ratio degradation of the converted signal which is attributed to the XGM effect in SOA-based devices [18]. As a result, the absorber will suppress the level of the spaces of the converted signal thus improving the extinction ratio along the cascaded stages of the buffer.

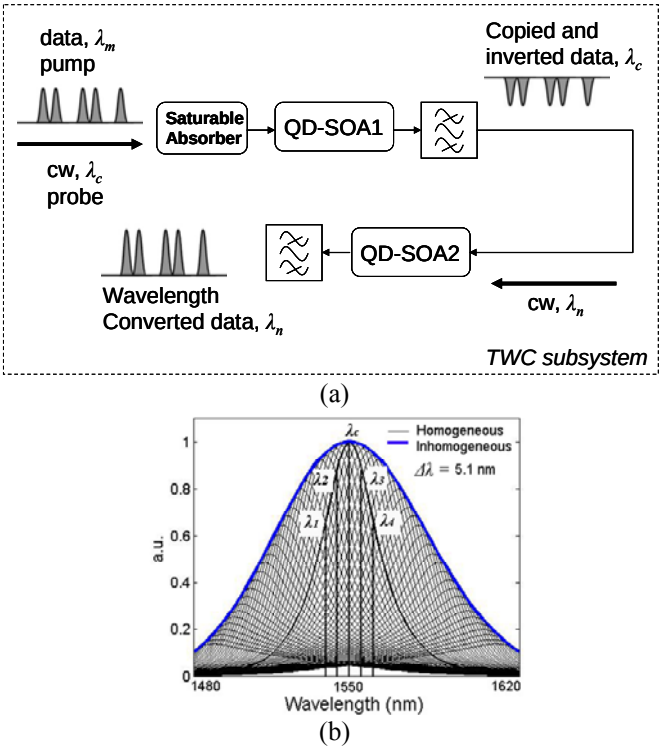


Fig. 5.3. (a) Configuration setup of TWC. (b) Available wavelengths for wavelength conversion lying within the single dot-group homogeneous broadening.

The buffer architecture is designed such as to exploit the maximum number of the available wavelengths which are symmetrically located around the center of the inhomogeneously broadened gain spectrum of the QD-SOA (Fig. 5.3(b)). However, it is necessary that all wavelengths are constrained within the spectral bandwidth of a single-dot group gain, known as the homogeneous broadening, for effective XGM to occur. In addition, the wavelength separation between adjacent wavelengths should be such that it prevents spectral overlap of the transmitted signals at 160 Gb/s.

The performance of the TWC subsystem cascade is based on extensive numerical analysis which simulates the carrier dynamics of the QD-SOA device. The implemented model is used to solve a set of rate equations each of which corresponds to the changes of the carrier density at each energy state of the quantum-dots: the ground state, the excited state, the continuum state and the wetting layer. The rate equations are presented in [19] The homogeneous single-dot group bandwidth is considered equal to 16 meV (~ 31 nm at 1550 nm communication window) at room temperature. The QD-SOA parameters have been obtained from [19], [20]. The available wavelengths $\lambda_{m,n}$ (m, n = 1, 2, 3, 4) are spaced at 5.1 nm around the central wavelength λ_c which is used for intermediate wavelength con-

version. Even if QD-SOAs have broad gain spectrum which is attributed to the size variation of the dots, only the spectrum under a homogeneous broadening can be exploited due to the fact that, XGM-based wavelength conversion should be feasible from an input available wavelength to an output available wavelength. In addition, for the simulation study that will follow, each tunable filter has been considered as a simple passive element of 2dB loss. Additional losses of 6dB have been considered for the MUX and DEMUX at the input and at the output of the TWC respectively, hence 8 dB losses have been considered for each TWC subsystem, in total.

The steady state response of the saturable absorber is simulated based on a simple transfer function which is introduced by the loss parameter $\alpha(t,P)$ that tracks the signal envelope according to $\alpha(t,P) = \alpha_0/(1+P(t)/P_{sat})$ [21], where P_{sat} is the saturation power and α_0 is the steady state loss being equal to -0.1 dB in this case. Extensive simulations have indicated an optimum value of +20 dBm for the P_{sat} parameter.

The input data consists of 32% duty cycle RZ-Gaussian pulses modulated by a 2^7-1 PRBS bit pattern at 160 Gb/s. The average input pulse power is 27 dBm and the cw probe power levels input to QD-SOA1 and QD-SOA2 are -15 dBm and 0 dBm, respectively. These values have been determined based on an optimization study in terms of the output extinction ratio and relative Q-factor ratio of the converted signal along the cascade of converters. The Q-factor ratio is directly related to the actual Bit-Error-Rate of the system, only when the signal degradation follows Gaussian statistics. Although in the present work this is not the case, this figure of merit function can still be used to reflect the efficiency of the converter illustrating its regenerative capabilities. In the present work and in order to highlight the regenerative properties of the TWC subsystem, the input data signal has 13 dB extinction ratio but suffers from amplitude jitter at the marks leading to input Q-factor 7. The length of SOA-based devices is an important parameter for their fast response and it has been previously studied and reported in the literature [22], [23]. Fig. 5.5.4 illustrates the gain recovery time of the QD-SOA as a function of the QD-SOA length at the impulse of very short pulses (500 fs) at 100 GHz repetition frequency. It is noteworthy that for lengths longer than 6 mm the gain response falls under 1ps indicating the applicability of QD-SOAs to high bit rate processing functionalities. It should be noted that experimental results have been published with up to 25 mm QD-SOA device [24]. The length of the QD-SOA device in the current simulation study is considered 10mm and the current density that drives the QD-SOAs is 36 kA/cm^2 in order to make sure that the upper layers are full of carriers.

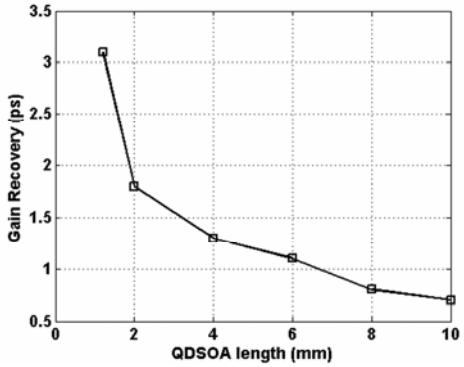


Fig. 5.4. QDSOA gain recovery time as a function of the device length.

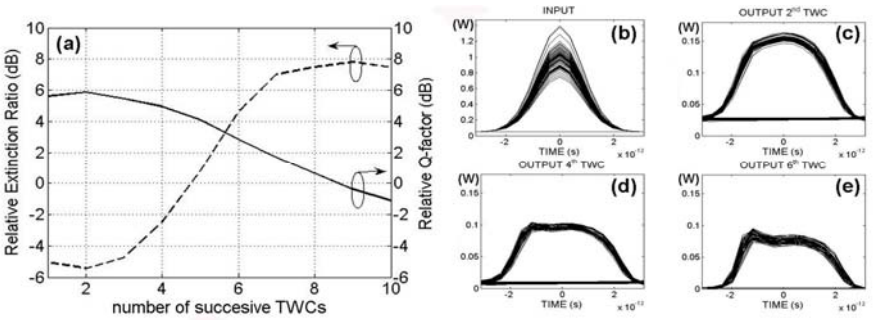


Fig. 5.5. (a) Relative extinction ratio and Q-factor ratio as a function of the number of successive TWCs (average values over 10 iterations). (b-e) eye diagrams of the input data signal and the converted data signals after the first, second and third stage of the buffer (worst case scenario out of 10 iterations).

Fig. 5.5.5(a) illustrates the relative extinction ratio and the Q-factor ratio of the converted signal with respect to the input values, after each TWC. The results depicted here are the averaged over 10 iterations. It is clear that, there are regions where both the extinction ratio and the Q-factor ratio show significant improvement. However, there is an inverse relationship between them as the number of successive converters increases imposing a trade-off. In particular, the extinction ratio gradually improves along the cascade reaching 8 dB at the output of the eighth TWC. On the contrary, the Q-factor ratio reaches 6 dB at the output of the first TWC, back tends to drop back to its input value at the output of the ninth TWC.

The worst case scenario out of ten iterations illustrating wavelength conversion from λ_1 to λ_4 and so on and so forth has been considered. Fig. 5.5.5(b-e), illustrate the eye diagrams of the input signal and the converted output signals after the first, second and third stage (second, fourth and sixth TWC). It is clear that, the level of spaces is suppressed owing to the saturable absorber. In addition, power overshooting at the leading edge of the pulse is observed which is attributed to self-

phase modulation effects in the QD-SOA [21]. At the output of the third stage of the buffer architecture, the extinction ratio and Q-factor improvement is 5dB and 3dB, respectively, illustrating the regenerative performance of the TWC subsystem. Finally, according to the equation which relates the number of cascaded stages with the number of packets served, we reach the conclusion that, under the aforementioned conditions, for 3 cascaded stages 9 input packets can be served.

5.3 Multiwavelength optical buffers

5.3.1 New buffer architectures

In this Section we use a QD-SOA based design, combing with an array waveguide grating router to transform multi-wavelength conversion to functional switching operations. Such a configuration is shown in Fig 5.6. It can be seen that packets from different inputs operate on different set of wavelengths. For example a packet from input 1(wavelengths: λ_1^{I}, $\lambda_1^{II,}$ $\lambda_1^{III,}$,λ_1^{IV}) may be converted only to wavelengths λ_1^{I}, λ_1^{II}, λ_1^{III}, or λ_1^{IV}. Thanks to that, all the signals may be converted and then transmitted in one shared fibre simultaneously. One of the other interesting functions of QD-SOAs and SOAs in general is that they can copy one signal to more than one wavelengths, when multiple probe signals are used [25]. This feature can be used for multi-casting purposes on packet per packet based within such optical switches.

In [26] we proposed 2 architectures for implementing optical buffers. Both use multi-wavelength selective elements like QD-SOAs as multi-wavelength converters and fixed-length delay lines that are combined to form both an output queuing and a parallel buffer switch design. The output queuing buffer design requires less active devices (QD-SOA) when implementing large buffers, but the parallel buffer design becomes more profitable, when the number of wavelength channels that can be simultaneously processed by the wavelength selective switches (QD-SOAs) increases.

The “parallel buffer” architecture is depicted in Fig 5.7. We have assumed a 4×4 switch, where an input stage (not shown in the figure) converts all input signals to four different ($\lambda_1 \ldots \lambda_4$) wavelengths. The main buffer stage of the size equals to 15 time slots consists of QD-SOAs followed by cyclic arrayed waveguide gratings (AWG) with banks of fibre delay lines (FDLs) at theirs outputs. To this end, for each input wavelength a set of four output wavelengths exist, equal to the AWG ports. Thus, a total of 16 internal wavelengths are needed (see Fig. 5.5.6). The first and the second QD-SOAs on the packet route simultaneously convert all packets from all the four wavelengths to four different internal wavelengths in order to access the desirable delay in the following banks of FDLs. In

the sequence, a third QD-SOAs acting as the output switch fabric forwards the data signals to the desired output link.

The packets from the different inputs operates on different set of wavelengths (Fig. 5.5.6), so the packet contention within the buffer doesn't occur. However, the contention problem arises when two or more packets from the same input (go to different outputs) arrive to the same QD-SOA simultaneously. In the "*parallel buffer*" architecture, it doesn't take place in the buffering stage but could appear in the output switching stage (the third QD-SOA on the packet route). To overcome such a packet contention, a simple scheduling algorithm given in the next section is proposed.

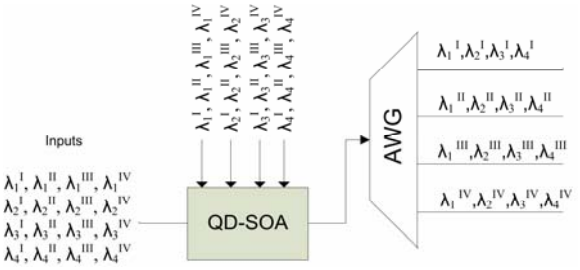


Fig. 5.6. QD-SOA acts as a multi-wavelength converter.

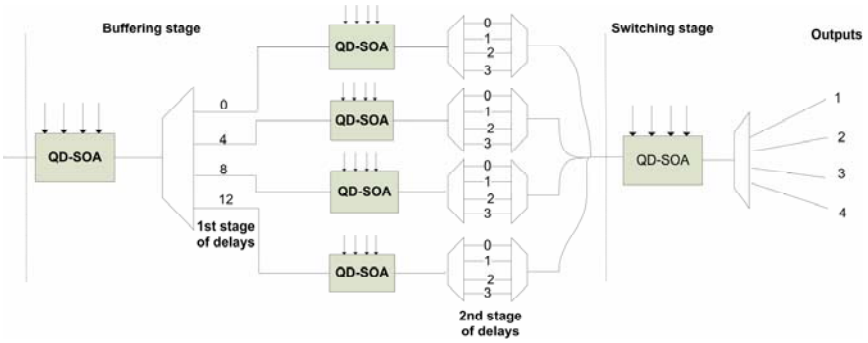


Fig. 5.7. The first and the second QD-SOA on the packet route simultaneously convert all packets from all the four wavelengths to four different internal wavelengths in order to access the desirable delay in the following banks of FDLs. In the sequence, a third QD-SOAs acting as the output switch fabric forwards the data signals to the desired outgoing link.

5.3.2 Scheduling algorithms

In this section a simple scheduling algorithm according to "parallel buffer" scheme is presented. It is based on the algorithm [27],To visualize a possible packet contention, let us consider the example shown in Fig. 5.5.8. We assume that packets are of fixed size and their duration is one time slot. All packets share

the same fibre delay lines so, it is not visible in the figures from which input and to which output come packets. The route of the specific packet is indicated by bolding the proper delay lines. Each delay line owns also a corresponded "number" mark which stands for its time slot delay. We assume that, some of the delay lines has been yet occupied thus, the starting point of our consideration is a x^{th} timeslot.

In such a time slot, only one packet – $P_{1,2}$ (from the first input to the second output) appears at the input of the switch. The next timeslot when the second output is free is $x + 8$, thus the packet delay is set to 8 timeslots. It goes then through the third branch and enters the first delay line. Six time slots later, packet $P_{1,4}$ enters the switch. In $(x + 8)^{th}$ time slot both packets enter the switching stage. The QD-SOA at the switch output that is commissioned to convert the signals back to their original wavelengths cannot serve two signals from the same input at the same time and thus a case of *wavelength contention* will occur.

It is also possible that more than two packets will compete in the last QD-SOA. To overcome the packet contention issue we may use more internal wavelengths or a simple scheduling scheme described below.

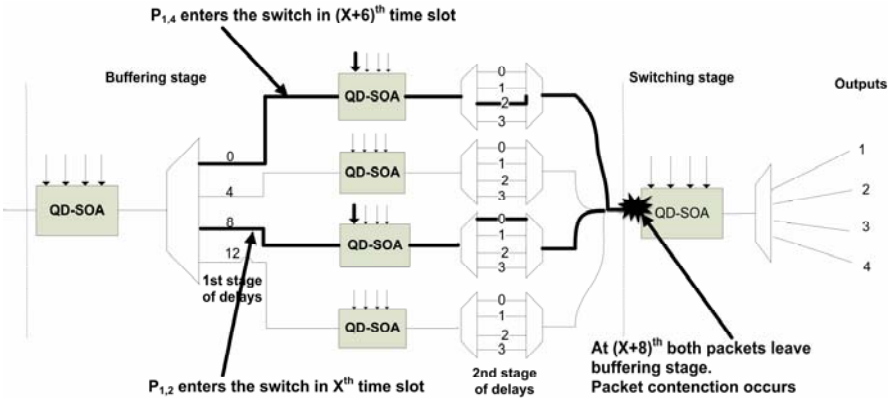


Fig. 5.8. The packet contention in the switch with parallel optical buffers. Both packets leave buffering stage at the same time slot and the packet contention appears on the input of the third QD-SOA.

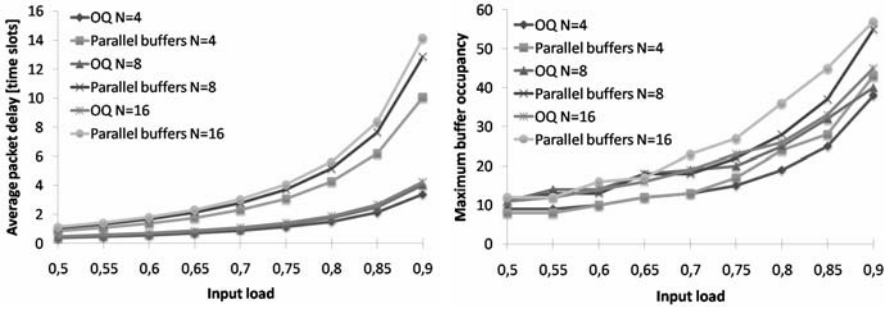
Every input is represented with a single- dimension matrix (vector). The length of each input vector equals a buffer depth + 1 (0^{th} timeslot means that packet will be sent immediately, without entering the delay line). Every cell within it, is a boolean value and corresponds to relevant timeslot. If the input is sending the packet out in X^{th} time slot, the X^{th} cell value in the vector must be set to 1.

In addition, every output owns a similar vector that indicates whether packets will be sent through this output in an appropriate time slot or not. A scheduling algorithm should prevent packet contention. In proposed structure, the scheduling algorithm must to choose the first time slot when both input and output are free.

This time slot is considered as a buffering time and then packets go to relevant delay lines. Contention can be resolved with a simple OR logic function. In particular, when a packet enters the X^{th} input, trying to reach Y^{th} output, the values corresponded to the same time slot in the X^{th} input vector and Y^{th} output vector will be considered and OR function will be executed. We assume a 15 timeslot buffer, so that the number of cells in each input (or output) vector is 16 (0-15 timeslots). The algorithm runs until the result of the OR function takes zero, which means in such a time slot both input and output are free and it is possible to send the packet without contention. Next, the values in the X^{th} input vector and Y^{th} output vector corresponded to the chosen time slot have to be set to one. When the algorithm has been executed $(N + 1)$-times, where N is the length of the buffer and the result of OR function is still one, the packet will be lost. In the next time slot all cells are shifted left.

5.3.3 Performance evaluation

In the simulation experiments we compared few performance metrics of the *parallel buffer* switch architecture and the output queued (OQ) switch. We considered the Bernoulli arrival model, where packets arrive at each input in the slot-by-slot manner. Under the Bernoulli process, the probability that there is a packet arriving in each time slot is identical and independent of any other slot. The probability that a packet may arrive in a time slot is referred to as the load of the input. The experiments have been carried out for a wide range of traffic loads: from 0.05 to 0.9 with the step 0.05. Time proceeded the exact simulation was 10000 cycles and exact simulation lasts 90000 time slots.



(a) (b)

Fig. 5.9. Comparison of (a) average packet delay and (b) maximum buffer occupancy for $b = \infty$, versus input load for different switch sizes.

We have evaluated the following performance metrics: the maximum occupancy of the buffer and a mean packet delay in case of an infinite buffer size (buffer size is denoted by b) as well as the packet loss probability (PLP) and mean packet delay when buffer size becomes 15, 31 and 63. The "parallel buffer archi-

tecture" suffers from a higher mean packet delay and maximum buffer occupancy than OQ switch model. It is worth noting that in case of the parallel buffer architecture with $b = \infty$; (see Fig. 5.5.9) and for loads lower than or equal to 0.7, the mean packet delay was less than 3 time slots, which can be considered to be satisfactory. For workloads less than 0.85, the mean delay does not exceed 8 time slots. Maximum buffer occupancy for N=16, in case of output buffered switch was found to be 57 packets.

In the "parallel buffer" architecture it is possible to implement 15 time slots buffer using a limited number of QD-SOAs. This is crucial to optical switching systems because the optical signal suffers from OSNR degradation. In the proposed architecture, the total number of QD-SOAs is five but the optical signal has to go only through two devices. This case applies when assuming a 4×4 switch and thus the input signal consists of $w = 4$ different wavelengths. Alternatively, the proposed switch architecture could be cascaded to employ more stages [26].

In the case of the switch with a large number of inputs/outputs, processing time of this algorithm may be too slow because every input has to match a free timeslot to send a packet, one after another (not simultaneously). Thus, considering large switches, it is also possible to use other scheduling algorithms [28] to solve a packet contention in "parallel buffer" architecture.

5.4 Multi-stage optical switches with optical recirculation buffers

5.4.1 The switching fabric architecture

Many proposed all optical switches suffer from limited scalability. A solution is to employ multistage Clos network architectures [29]. The three-stage Clos-network architecture is denoted by *C(m, n, k)*, where parameters *m, n*, and *k* entirely determine the structure of the network. There are *k* input switches of capacity $n \times m$ in the first stage, *m* switches of capacity $k \times k$ in the second stage, and *k* output switches of capacity $m \times n$ in the third stage. The capacity of this switching system is $N \times N$, where $N = nk$.

A multistage switching network is called strictly nonblocking when it is always possible to connect any idle input port to any idle output port irrespective of other connections set up in the network. A switching network is rearrangeable nonblocking if it is possible to connect any idle input port to any idle output port, but some of the existing connections have to be reconfigured to do so. A switching network is called internally blocking when it is not able to guarantee connection

between an idle input and an idle output. The three-stage Clos-network switching fabric is strictly nonblocking if $m \geq 2n-1$ and rearrangeable nonblocking if $m \geq n$.

In a packet switching concept, like optical packet switching (OPS), time-sliced optical burst switching (TSOBS), and optical cell switching (OCS) the switch adopts a slotted mode of operation. In one time slot packets form the input side are switched to the appropriate outputs, therefore in the next time slot the switch may be completely reconfigured. In this case it is sufficient to have a rearrangeable nonblocking switch, because in each time slot we can choose other second-stage switch [30]. In all-optical switching schemes time is divided into fixed size slots. In each time slot we can send one optical packet called cell. While a cell is being routed in a packet switching system, it can face a contention problem resulting from two or more cells competing for a single resource. In terms of place, where the contention points occur it is possible to categorize the contention states into output port contention and internal contention (internal blocking) [31]. In general, there are three ways to avoid collisions i.e. optical buffering, optical wavelength conversion and deflection routing [32], [33]. Using optical buffering strategy would make the structure of an optical switch strictly close to that of a traditional electronic packet switch, therefore it is extensively investigated. Since the optical RAM buffer is not available yet, the only practical optical buffers today are fibre delay lines (FDLs), which are fixed-length fibres. A packet which has entered the fibre must emerge from the other end after a fixed amount of time and cannot be removed before that time. The implementation of large buffers requires a large number of fibre delay lines of different length and causes a high hardware cost. The fibre loop memory may be also used for buffering (delaying) cells when contention occurs. The contending packet is pushed into the loop on the available wavelength after converting it through tunable wavelength converter. The storage time is equal to the number of recirculations.

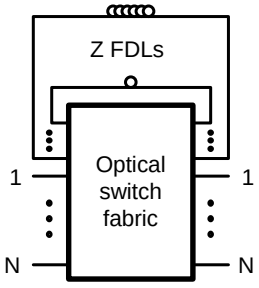


Fig. 5.10. Shared-FDL switch.

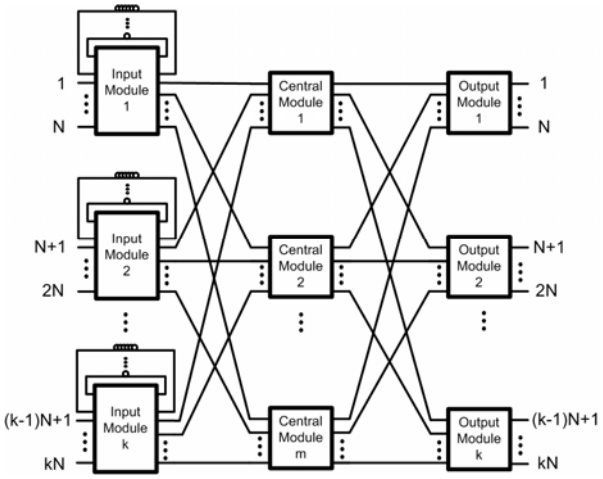


Fig. 5.11. Three-stage shared-FDL-IM optical Clos-Network

switch.

The architecture of the single-stage shared-FDL switch was first proposed by Karol in [34] (Fig. 5.5.10). The switch called Shared-Memory Optical Packet (SMOP) Switch uses feedback FDLs to resolve packet contentions and can achieve good performance with proposed control algorithms.

The switch has N input ports, N output ports and Z feedback FDLs of appropriately-selected length, that are shared by all input ports. The optical switching fabric used within the SMOP Switch is memoryless, rearrangeable non-blocking e.g. an optical crossbar switch fabric and has a $(N + Z) \times (N + Z)$ dimension. The lengths of the delay lines could be: d_1, d_2, d_3, …, d_m packet duration (slots). A total of $B = (d_1 + d_2 + d_3 + \ldots + d_m)$ packets can be stored in the recirculation fibres. This reduces to $B = m(m+1)/2$ when $d_1 = 1$, $d_2 = 2$, $d_3 = 3$,…, and $d_m = m$. Each FDL delays cells by a fixed number of time slots, and in general, any two FDLs may have the same or different delay values. Delay lines of length greater than one packet duration reduce the number of recirculation loops needed. As a result the number of amplifiers may be reduced and less noise is added to the signal. Another limitation is that each FDL requires one switch port, thereby increasing the overall switch cost with increased number of FDLs. In the case of two or more cells collision only one of them gets access to the output port and the others are routed to the available FDLs according to how much delay each packet needs. A packet that is buffered in a loop of length d_i will exit the delay line after d_i time slots. The scheduling algorithm selects packets to be sent to outputs, and also assigns the remaining packets to the recirculation loops. The required delay of k time slots for the particular packet may be achieved by buffering it in a recirculation delay line of length k (if possible) or by combinations of delay-line lengths that sum to k. The scheduling decisions may be revised each time a packet returns to the optical switch fabric from the feedback loops e.g. new higher priority packets may be transmitted without delay.

5.4.2 Scheduling algorithms for the single-stage shared FDL switch

In [34] Karol has proposed two scheduling schemes called non-FIFO and FIFO respectively. The non-FIFO algorithm does not attempt to keep packets in their proper first-in, first-out sequence, while the FIFO algorithm is more complex and maintains FIFO packet sequence. Both proposed algorithms cannot guarantee that packets that are lost in the contention and have to be buffered can get access to the desired output port after coming out from the FDLs. Therefore, the number of packet recirculation is unpredictable in advance. Minimum delay can be achieved by giving the higher priority to the packet that comes out from the longest FDL. The simulation results published in [34] show that the maximum number of recirculations required in Karol's algorithm can be as high as 10. This is undesired

since the optical signals will be significantly attenuated with such number of recirculations.

Three FDL assignment algorithms for the single-stage shared-FDL optical switch, namely sequential FDL assignment (SEFA), multicell FDL assignment (MUFA), and parallel iterative FDL assignment (PIFA), were proposed by S. Y. Liew et al. in [35]. These algorithms alleviate the recirculation problem by the implementation of FDLs and output port reservation. The algorithms can make the output port matching for current time slot and the FDLs assignment for the entire journey of a delayed packet so that it can be scheduled to match with the desired output port in the future time slot. The number of packet recirculation here depends on the maximum number of FDLs. If the FDLs are unavailable and the packet fail to be scheduled it will be discarded before entering the switch to avoid any FDL resources occupation.

The SEFA algorithm searches FDL routes for cells in a cell-by-cell basis, so the cells which arrive in the same time slot are scheduled one after another. The decisions are taken on the basis of a configuration table which is maintained by the shared FDL switch. The configuration table is used to making all possible FDL routes and indicating the switching schedule of the switch. It can be formulated into a slot transition diagram that includes all possible FDL routes for cells. The MUFA algorithm uses sequential search to assign FDLs for multiple cells simultaneously. The algorithm also maintains the configuration table as in SEFA algorithm, but the slot transition diagram is modified to guarantee that the FDL routes with fewer delay operations are searched and assigned for cells earlier. The PIFA algorithm uses a distributed method to assign FDL routes for multiple cells simultaneously. The same modified slot transitions diagram as for the MUFA algorithm is used. The simulation results concerning the SEFA, MUFA and PIFA algorithms are presented in [35]. To avoid packets out-of-order problem X. Wang at al. have proposed and evaluated modified MUFA algorithm called SMUFA (Sequence MUFA) [36].

5.4.3 Scheduling algorithms for the three-stage shared FDL optical clos-network switch

The three-stage optical Clos-network switch (OCNS) is a potential solution to overcome the limited scalability of single-stage switches. In general, the FDLs can be placed at the input modules (IMs), central modules (CMs) and/or at the output modules (OMs). Different FDL location influencing scheduling complexity and performance. The three-stage optical Clos-network switch with FDLs placed at IMs is shown in Fig. 5.5.11. In this kind of the optical Clos-network cells may be delayed only at the first stage, while the second and third stages are used only for switching.

Two assignment algorithms for the OCNS were proposed by S. Jiang in [37] namely sequential FDL assignment algorithm for Clos-network switches (SEFAC) and multicell FDL assignment for Clos-network switches (MUFAC). The former assigns FDL routes and determines central-module routes in the Clos-network at a cell-by-cell basis, while the latter assigns FDL routes for multiple cells simultaneously and then assigns central-module routes in a heuristic manner.

In the SEFAC algorithm each input module maintains its own slot transition diagram, while the whole system maintains a configuration table to check the availability of all outputs in each time slot. For each input port it is necessary to find the earliest time slot that satisfies the following three conditions: (1) the destined output port is idle in the time slot; (2) on the corresponding input module there is the FDL route which can delay the cell to that time slot; (3) a connecting path between the input module and required output module is available at the time slot.

If there is possible to find the time slot that fulfill these three conditions, the SEFAC algorithm assigns the FDL route, departure time, and randomly selects available central-module of the three-stage optical Clos-network for set up the connecting path to the desired output port. For each input port the searching process is performed sequentially and in addition the round robin mechanism is employed for selection of an input module with the highest priority for the searching process.

The MUFAC algorithm is a modification of the MUFA algorithm and it can assign FDL routes and departure times for multiple cells simultaneously in a distributed manner. It has to perform three steps: (1) assignment of FDLs routes in the IMs; (2) scheduling cell departure times according to the output port availability; (3) assignment of connecting path between input modules and output modules for multiple cells in the same time slot.

The heuristic algorithm proposed by M. Karol in [40] is used in MUFAC scheme for set up connecting paths between input modules and output modules in three-stage optical Clos-network switch. The optimized algorithms provided guaranteed routes for all matches were proposed in [38], [39].

The MUFAC scheme is based on transition diagrams maintained by each IM, where each level-k node keeps information about available FDLs of that IM for time slot t. In addition, each OM keeps information about availability of their output-ports, and each of the IMs and OMs keeps the corresponding connecting path availabilities. The FDL assign process uses the transition diagram to find one or more delay lines to delay cell to required time slot n.

In the next step the MUFAC algorithm attempts to pair up each IM to a particular OM using Karol's matching algorithm. After this step there are k IM-OM pairs and only between these matched modules it is possible to send cells. The algorithm has to go through four phases namely request, grant, accept and update to select cells to be sent to output ports. The request phase is performed independently in each IM. In this phase the parent node sends the unfulfilled requests to its child nodes, and each child node collects information about availability of the output port from the paired OM for the corresponding time slot. This information is

used in the grant phase to grant unfulfilled requests with the available output ports. In the next step grant decisions are sent back to the parent node. The parent node collects the central routes availabilities from the corresponding IM and the paired OM. The accept decisions made by the parent node are based on the following criteria: (1) unfulfilled input port requests; (2) availability of FDL on that IM for the corresponding time slots; (3) availability of connecting paths from that IM to the paired OM in the corresponding time slots; (4) in the case of several grants, the parent node accepts the grant with the earliest departure time. At the end of the accept phase a parent node passes the accept decision to its child nodes for updating. In the update phase, the parent node updates central route and FDL availabilities, while the child nodes update output port availabilities on paired output module. All phases mentioned above can be executed in a distributed manner.

5.4.4 Simulation experiments

The performance of SEFAC and MUFAC algorithms was evaluated using computer simulation. The three-stage optical Clos-network switch of size 1024×1024 with FDLs placed at IMs was considered in simulation experiments (the same architecture as in [37]). The investigated switching network consists of 32 IMs, 32 CMs, and 32 OMs of capacity 32×32. Each IMs employs 32 FDLs, and there are 5, 5, 5, 5, 4, 4, and 4 FDLs with delay values 1, 2, 4, 8, 16, 32, and 64 cell times respectively. We have carried out the simulation experiments also for doubled number of FDLs (64) at each IM. The delay operation for each cell was limited to two in SEFA as well as in MUFA algorithms. The Bernoulli arrival model and uniform traffic distribution pattern are considered in simulation experiments. Two performance measures were evaluated: the average cell delay in time slots and cell loss rate. The simulation results are shown in Fig. 5.5.12 and Fig. 5.13.

We can see that both FDL assignment algorithms proposed for the three-stage optical Clos networks switch with FDLs placed at IMs can achieve $\sim 10^{-8}$ loss rate at 0.86 input load (Fig. 5.5.12). The results obtained for both algorithms are compatible for the case with 32 FDLs at each IM. It is possible to observe that the SEFAC algorithm performs better at a load below 0.94, while the MUFAC algorithm performs better at a load above 0.94. The results are a little bit different when 64 FDLs are employed and the better results gives the SEFAC algorithm. For the large number of FDLs the SEFAC algorithm uses the FDLs more efficiently than the MUFAC algorithm.

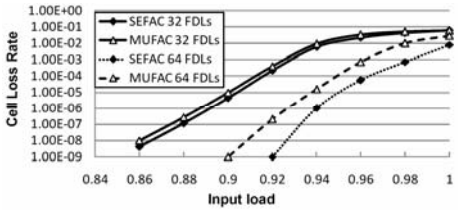


Fig. 5.12. Cell loss rate for SEFAC and MUFAC; 32 and 64 FDLs at each IM.

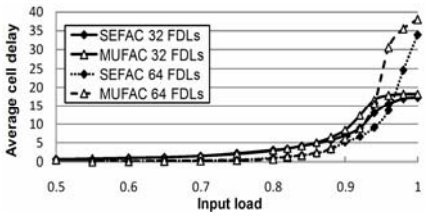


Fig. 5.13. Average cell delay for SEFAC and MUFAC, 32 and 64 FDLs at each IM.

The average cell delay for both algorithms is very low for wide range of input load and do not exceed 20 for very high input load – close to 1 in the case with 32 FDLs at each IM (Fig. 5.5.13). We observed that for input load greater than 0.88 the SEFAC algorithm gives slightly lower average cell delay than the MUFAC algorithm. For 64 FDLs at each IM and input load greater than 0.9 the average cell delay grows faster for MUFAC than for SEFAC, but do not exceed 40 and 30 cells respectively. This result is obvious due to lower cell loss rate for the case with 64 FDLs at each IM. Note that under heavy input traffic load the cell delay factor depends also on availabilities of connecting paths between IM and OM. The heuristic algorithms used in simulation experiments become also a recourse limitation.

Taking into account the time complexity it is necessary to emphasize that MUFAC is more feasible than SEFAC. The MUFAC algorithm can handle multiple packets at the same time and is scalable, while SEFAC has scalability limitation mostly due to time complexity, which is in linear proportion to the switch size. The time complexity of SEFAC as well as MUFAC was evaluated in [37].

5.5 Optical asynchronous packet switch architectures

5.5.1 All-optical buffer technologies

To implement an optical memory using current technologies, we believe that two methods are practically relevant, namely the one based on electromagnetically induced transparency EIT and one based on coupled cavity waveguides.

5.5.1.1 Electromagnetically induced transparency

When light interacts with a three atomic energy levels it is possible to observe electromagnetically induced transparency. This effect allows for using one optical field to control the absorption and dispersion of another optical field. More pre-

cisely, by varying the intensity of the controlling field it is possible to drastically modify the group velocity of a signal beam. The group velocity is given by:

$$v_g = \frac{c}{1 + \frac{g^2 N}{\Omega_c^2}} \tag{5.1}$$

where g is the coupling constant for the signal beam, N is the density of the medium, and Ω_c is the Rabi frequency for the control field. Thus, very small group velocity can be achieved by decreasing the control field intensity. Also, by adiabatically reducing the control field to zero the effective group velocity becomes zero, accompanied by storage of the light pulse as a material excitation. This has been observed in cold atomic gases, hot gases, and in doped crystals. The allowed storage time is determined by the coherence of the involved atomic levels, i.e. how well one can keep a quantum mechanical superposition of the atomic states. This coherence time is determined by the particular choice of material and the environment of the medium. States encoded in cold atomic gasses are the most robust allowing storage times up to 1 ms. For doped crystals where the environment is more uncontrollable, storage times up to 100 μs has been observed at cryogenic temperatures.

For practical use of electromagnetically induced transparency (EIT) in telecommunication systems it is not favourable to use alkali metals, such as rubidium or sodium where the effect has been demonstrated. The reason for this is that optical transitions for these atoms are far from wavelengths suitable for optical communication (1.3-1.5 μm). Atoms are also not subject to engineering, so it is difficult to engineer optical components based on atomic transitions, so one either adapt other components to suit the used atom, or one is lucky enough to find an atom that has the desired transitions. These two inflexibilities seem to imply that atoms will remain highly impractical to use as the active medium at the telecommunication wavelengths. The doped crystals are also unsuitable for practical applications because of the low crystal temperatures involved. For a successful implementation of a three-level system required by EIT one needs an optically active material with absorption in this interval with good coherence properties. There are plenty of semiconductor materials and structures with suitable optical transitions in this wavelength interval. These are frequently used to build lasers, modulators etc. Unfortunately, all these materials and structures have exceptionally poor coherence properties compared to the alkali atoms, so any application relying on a semiconductor implementation would have to operate at timescales faster than the decoherence time. For atoms, the coherence times are around seconds at room temperature, which is significantly longer than for any semiconductor material where the coherence rarely exceeds seconds, even at low temperatures. Error correction could in principle be used to increase the coherence time of semiconductor systems, but this remains experimentally untested.

For an atomic implementation of EIT, there is one atom that is usable at telecom wavelengths. The lutetium atom (175Lu) has a ground state consisting of hyperfine levels (F=2, 3, 4, 5) with electronic configuration [Xe]5d16s2 (2D3/2). The main transition of this atom occurs at the wavelength 1.337 μm to the state [Xe]6s26p1 (2P3/2). This transition fulfils all the requirements needed for an implementation of EIT. These transitions are within the O-band (1.260-1.360 μm) used for some telecommunication systems. The allowed storage time is determined by the coherence of the involved atomic levels, i.e. how well can one keep a quantum mechanical superposition of the atomic states. Expressed in another way, the storage time is roughly equal to the time the two (e g atomic) states storing the optical pulse can retain their relative phases. The performance of EIT based optical signal processing schemes, such as an optical delay line or buffer, depends on the coherence between the atomic levels.

The most realistic semiconductor system would be quantum dot arrays. These would have the advantage that the coupling constant for the optical interaction is much larger than for the atoms. In addition the coherence properties are among the best for the semiconductor systems. Also, the quantum dots can be integrated with other opto-electronic components using standard semiconductor technology.

5.5.1.2 Coupled cavity waveguides

Another promising candidate for an optical memory is to use a coupled cavity waveguide where the light may couple into auxiliary cavities next to the waveguide. This approach has the advantage that the cavities can be microfabricated and engineered for specific applications. To obtain storage times much longer than 50 ns will be a challenge using existing technologies and at the same time keep the device small. Therefore, also the cavity scheme is suitable only for high-speed systems that require short storage times. In the cavity storage scheme, it is necessary to control the coupling strength between the different cavities to switch the device from a guiding mode to a storing mode. Such switching can be performed either using electro-optic elements, or mechanical/thermal positioning of the cavities. This will unfortunately increase the device complexity.

5.5.2 Node architectures

5.5.2.1 Contention resolution based on hybrid buffers

The considered optical packet switching node has a capacity of $n \times N$ wavelength channels, where N is a number of input and output fibres and n is a number of wavelength channels multiplexed on each fibre. We show two architectures of the

optical asynchronous packet switching node with hybrid buffers (see Fig. 5.5.14 and Fig. 5.5.15) [41]. The first one, referred to as Structure I, is based on a dedicated output buffer while the second one, referred to as Structure II, is based on a shared buffer.

Structure I consists of $N \times 2N$ optical switch matrices, $N \times N$ buffer blocks, and $n \times N$ 2-to-1 optical switches. The buffer block consists of one pipeline buffer per output and wavelength. After passing the switching matrix, packets can either be terminated to the addressed output link or, if the output port is occupied, the packets are routed to the dedicated buffer. As soon as the corresponding output link is available packets from the buffer are sent directly to the output link. The optical 2×1 switches are to select a packet at the specific wavelength from either the switch matrix or from the buffer. This architecture is very simple and the pipeline is easy to control because no virtual queuing algorithms are needed.

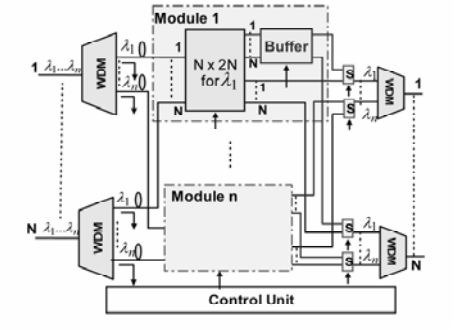


Fig. 5.14. Structure I.

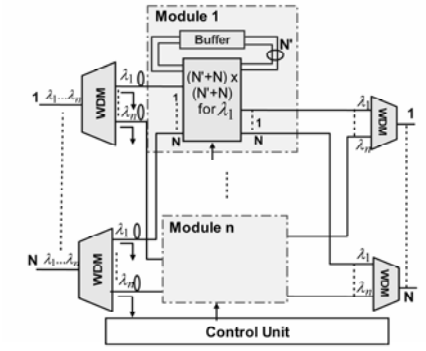


Fig. 5.15. Structure II.

The second architecture (Structure II) is based on $(N' + N) \times (N' + N)$ optical switch matrices and $N' \times N'$ buffer blocks. This structure allows for sharing the buffer resources. The buffer positions are not dedicated to the specific output links and can be shared by several channels. A number of parallel buffer positions (N') is offered per wavelength and is shared by all output ports (see Fig. 5.5.15). Structure II is more flexible, but it requires a more sophisticated control system. Shared, parallel memory requires advanced virtual queue management that has to be done by the control unit. It requires more complicated algorithms and more computing time.

For both node architectures the switch fabric can be divided into n identical modules. Each module serves one wavelength channel. The traffic load for a wavelength channel is assumed to be uniformly distributed between the outputs. Further, we assumed that the traffic load at all inputs is identical. These assumptions make evaluation of one module representative for the entire switch.

5.5.2.2 Contention resolution based on optical buffers and tunable wavelength converters

Fig. 5.5.16 and Fig. 5.5.17 [42] schematically illustrates the switch architectures A1 and A2. The switch fabric of A1 can be divided into n identical wavelength modules. Each module serves one wavelength channel and consists of a buffer block with b optical buffers and $(m + b) \times (2m+b)$ strictly non-blocking optical switch matrix. The wavelength conversion part of each module consists of m TWCs which are connected to all m output ports. Arriving packets are delivered to the addressed output fibre at the same wavelength if available. Otherwise, if another wavelength at the addressed output fibre is available, packets are sent to the TWC, converted to the available wavelength and delivered to the addressed output fibre. Since in A1 m TWCs are provided in each module (i.e., the same number as the input/output fibres) there will always be TWCs available if needed. However, if all the wavelengths at the addressed output fibre are occupied, packets are sent to the all-optical buffer block and wait until the appropriate output channel is available. If the time of packets stored in the buffer is longer than the maximum storage time of the optical buffer, packets are expired.

The switch fabric of A2 also can be divided into n identical modules. However, each module of A2 does not serve the specific wavelength, since the recirculation wavelength converters are attached to each switch matrix as shown in Fig. 5.5.17. Therefore, in A2 packets that have been converted to another wavelength pass the switching matrix twice. In the next section we evaluate how both the number of buffers b and the number of TWCs c can improve contention resolution at the node.

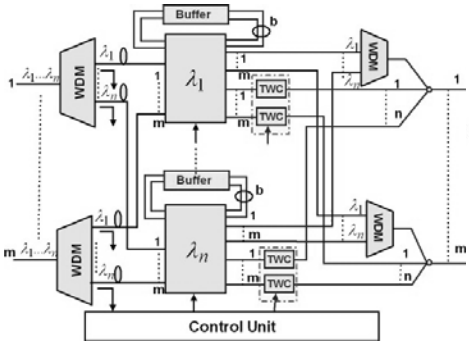


Fig. 5.16. OPS architecture A1 based on optical buffers and tunable wavelength converters

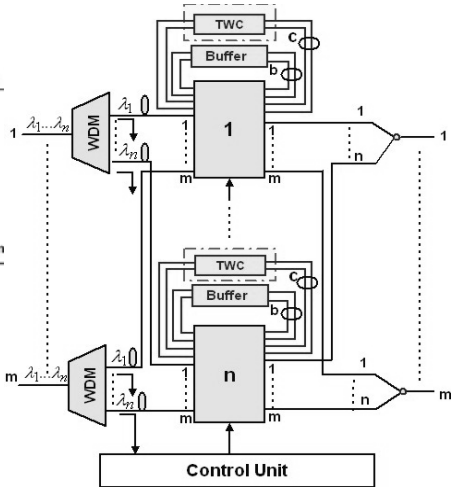


Fig. 5.17. OPS architecture A2 based on optical buffers and tunable wavelength converters

5.5.3 Performance evaluation

Switch performance has been evaluated through a computer simulation tool that allowed simulations of ATM (Asynchronous Transfer Mode) and IP traffic. For Structures I and II we study the benefits of implementing optical memory in the optical packet switching node in addition to electronic ones. In [43] it is shown that Structure I is less suited for this kind of evaluation due to the limited flexibility of the scheduling algorithm that can be applied. We proposed to add a few all-optical buffer positions to the electrical buffer block and evaluated the switching node based on the shared hybrid buffer.

We studied the admission algorithm giving a priority for the service that requires optical signal transparency in order to minimize the time a transparency packet has to spend in the buffer. We assumed that the load of this class of packets is 20% of the total load. The transparency packets were scheduled to be transmitted before the packets that could wait in the electrical buffer. In order to avoid non-priority packets waiting for ever, the transparency packets did not get the "total" priority. We implemented the following scheduling algorithm. If, at arrival of a transparency packets which need to be buffered, there are already packets in the electrical buffer waiting to be transmitted at the same output up to seven optical packets will be transmitted prior to the electrical and then packets will be transmitted in the order of arrival.

We have shown that the packet loss probability can be significantly improved by implementing a few optical buffer positions. At the same time a new optical memory technology allows for building an asynchronous optical packet switch with optical buffers. Furthermore, we evaluate architectures A1 and A2. The simulation results are presented in Fig. 5.5.18. It is shown that improvement achieved by TWCs is the higher, the larger optical buffer size is. Thus, for ATM traffic we can observe a boosting effect of caused by optical buffers. It is clearer for ATM traffic than for IP traffic. Furthermore, for IP traffic, packet loss probability less than 1%, which is often required, can be achieved only at low load (less than 30%) due to insufficient maximum storage time for IP traffic pattern while for ATM traffic packet loss probability passes the 1% level with a few buffer positions. It can be seen that for A2 increasing the number of TWCs above 8 does not make any improvement in the switch performance. It is due to small number of wavelengths on each fibre ($n = 4$) assumed for the simulations.

It should be noted that our results are very much dependent on the choice of parameters m, n and the maximum storage time. It is obvious that for smaller number of input/output fibres (m) the packet loss probability would be lower. Also, we would expect that if n/m increased (i.e. with lower number of input/output fibres and/or higher number of wavelengths per fibre) to a certain level, TWCs would become more efficient in solving congestion than optical buffers.

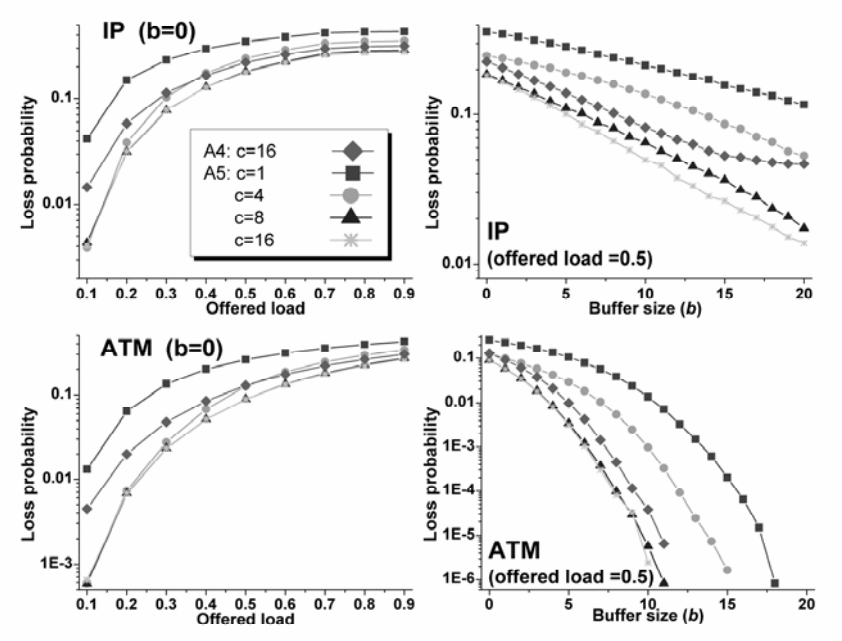


Fig. 5.18. Evaluation of A1 and A2. Packet loss probabilities for IP and ATM traffic patterns.

Our results reveal that A2 outperforms A1 with regard to number of TWCs, which is related to the cost of the switching node. However, one should take into account that fabrication of switching matrices for multiwavelenth operation can be more difficult and expensive than for one selected wavelength.

Finally, it should be mentioned that the two main advantages of our architectures for implementing in an optical packet switching network are: the asynchronous operation and relatively small optical buffer and number of TWCs needed to obtain low packet loss probability.

5.6 Conclusions

The new architectures of optical packet switches and optical buffers were studied in this Chapter. We have demonstrated the applicability of QD-SOAs in the realization of a 160 Gb/s line rate buffer architecture. Physical layer simulation results have shown regenerative performance in terms of extinction ratio and Q-factor improvement along the cascade of converters up to the third stage of the buffer. We have also considered applicability of QD-SOAs as multi-wavelength converters for constructing parallel optical buffers with high buffer depth and low number of wavelength converters. We have also discussed the switching fabric architecture of greater capacity, constructed from optical switches arranged in stages and

with recirculation buffering in the first stage. We have presented several scheduling algorithms for such architecture and shown by simulation that performance of these algorithm are sufficient for using them in practice. Finally, we have discussed two switch architectures with optical buffering, which enables the asynchronous operation. These architectures have been compared in the number of TWCs needed and the packet loss probability.

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